IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method for forming an electronic device comprising:

forming a first conductive layer in an opening in a dielectric structure supported by a substrate;

forming a core conductive layer on the first conductive layer, the core conductive layer having a top surface;

subjecting the core conductive layer to a H_2 plasma treatment; ~~and~~

depositing a capping ~~adhesion/barrier~~ layer on the core conductive layer after the H_2 plasma treatment, the capping layer to provide at least one property, the property selected from an adhesion property and a barrier property, the capping layer being conductive; and

processing the capping layer such that the capping layer completely covers the top surface of the core conductive layer substantially without being on areas surrounding the core conductive layer.

2. (Currently Amended) The method of claim 1, wherein forming a first conductive layer includes depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer, the base conductive layer to provide at least one property, the property selected from an adhesion property and a barrier property.

3. (Currently Amended) The method of claim 2, wherein depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

4. (Currently Amended) The method of claim 2, wherein depositing the seed layer and the capping ~~adhesion/barrier~~ layer includes depositing the seed layer and the capping ~~adhesion/barrier~~ layer using low energy ion implantation.

5. (Currently Amended) The method of claim 4, wherein depositing the seed layer and the capping ~~adhesion/barrier~~ layer using low energy ion implantation includes using an implant energy ranging from about 0.1 keV to about 2 keV.

6. (Original) The method of claim 1, wherein forming a core conductive layer includes depositing the core conductive layer using a CVD process.

7. (Original) The method of claim 1, wherein forming a core conductive layer includes forming the core conductive layer at a temperature ranging from room temperature to about 250°C.

8. (Currently Amended) The method of claim 1, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

9. (Currently Amended) The method of claim 1, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing the capping adhesion/barrier layer having a thickness ranging from about 5 Å to about 40 Å.

10. (Currently Amended) The method of claim 1, wherein the method further includes removing at least a portion of the dielectric structure, after depositing the capping ~~adhesion/barrier~~ layer on the core conductive layer, to form an air bridge structure.

11. (Currently Amended) The method of claim 1, wherein forming a core conductive layer and depositing a capping ~~adhesion/barrier~~ layer includes forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer in the opening in the dielectric structure, the dielectric structure having multiple dielectrics layers, such that the core conductive layer and the capping ~~adhesion/barrier~~ layer are within one dielectric layer in the dielectric structure with a top surface of the capping ~~adhesion/barrier~~ layer substantially level with a top surface of the one dielectric layer.

12. (Currently Amended) The method of claim 11, wherein forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer within one dielectric layer includes forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer within a polymer layer, a foamed polymer layer, a fluorinated polymer layer, a fluorinated oxide layer, or an aerogel layer.

13. (Withdrawn) A method for forming an integrated circuit comprising:

forming one or more device structures on a substrate;

forming a polyimide layer above a number of first level vias provided for electrical coupling to at least one of the one or more device structures;

forming a number of trenches in the polyimide layer;

forming a first conductive layer in the number of trenches;

depositing a core conductive layer on the first conductive layer, the core conductive layer having a top surface;

subjecting the core conductive layer to a H_2 plasma treatment; ~~and~~

depositing a capping ~~adhesion/barrier~~ layer on the conductive layer after the H_2 plasma treatment, the capping layer to provide at least one property, the property selected from an adhesion property and a barrier property, the capping layer being conductive, wherein a top surface of the capping ~~adhesion/barrier~~ layer is substantially at a top surface of the polyimide layer; and

processing the capping layer such that the capping layer completely covers the top surface of the core conductive layer substantially without being on areas surrounding the core conductive layer.

14. (Withdrawn) The method of claim 13, wherein forming a first conductive layer includes depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer, the base conductive layer to provide at least one property, the property selected from an adhesion property and a barrier property.

15. (Withdrawn) The method of claim 14, wherein depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

16. (Withdrawn) The method of claim 13, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing material by ion implantation into the core conductive layer to form the capping ~~adhesion/barrier~~ layer.

17. (Withdrawn) The method of claim 13, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

18. (Withdrawn) The method of claim 13, wherein forming a polyimide layer above a number of first level vias includes:

forming a field oxide layer and a Si_3N_4 layer above the one or more device structures;

forming contact holes through the field oxide layer and the Si_3N_4 layer;

depositing TiN in the contact holes;

forming tungsten on the TiN to form a contact plug; and

applying the polyimide on the Si_3N_4 layer and contact plug.

19. (Withdrawn) The method of claim 13, wherein forming a number of trenches in the polyimide layer includes:

forming an oxide layer on the polyimide layer;

forming a layer of Si_3N_4 on the oxide layer;

forming a damascene image in the oxide and Si_3N_4 layers; and

removing polyimide at locations of the damascene image.

20. (Withdrawn) The method of claim 19, wherein the method further including removing the layer of Si_3N_4 using a selective etch after forming the first conductive layer, and after

depositing the capping ~~adhesion/barrier~~ layer subjecting the oxide layer to an etchant that removes the oxide layer without substantially altering the polyimide layer.

21. (Withdrawn) The method of claim 13, wherein depositing a core conductive layer includes selectively depositing copper.

22. (Withdrawn) The method of claim 13, wherein depositing a core conductive layer includes selectively depositing the copper by plating in an ambient air environment.

23. (Withdrawn) The method of claim 13, wherein depositing a capping ~~adhesion/barrier~~ layer on the core conductive layer includes implanting zirconium ions into the core conductive layer.

24. (Withdrawn) The method of claim 13, wherein forming a polyimide layer includes forming a foamed polyimide, a fluorinated polyimide, or a foamed fluorinated polyimide.

25. (Withdrawn) The method of claim 13, wherein the method further includes a heat treatment at a temperature ranging from 250°C to about 350°C for a period ranging from about one hour to about two hours after depositing ~~an adhesion/barrier~~ the capping layer on the core conductive layer.

26. (Withdrawn) The method of claim 13, wherein the method further includes removing at least a portion of the polyimide layer, after depositing the capping ~~adhesion/barrier~~ layer on the core conductive layer, to form an air bridge structure.

27. (Withdrawn) A method for forming an integrated circuit comprising:

forming one or more device structures on a substrate;

forming a first oxide layer above a number of first level vias for electrical coupling to at least one of the one or more device structures;

forming a number of trenches in the first oxide layer;

forming a first conductive layer in the number of trenches;

depositing a core conductive layer on the first conductive layer, the core conductive layer having a top surface;

subjecting the core conductive layer to a H_2 plasma treatment; ~~and~~

depositing a capping ~~adhesion/barrier~~ layer on the core conductive layer after the H_2 plasma treatment, the capping layer to provide at least one property, the property selected from an adhesion property and a barrier property, the capping layer being conductive, wherein a top surface of the capping ~~adhesion/barrier~~ layer is substantially at a top surface of the first oxide layer; and

processing the capping layer such that the capping layer completely covers the top surface of the core conductive layer substantially without being on areas surrounding the core conductive layer.

28. (Withdrawn) The method of claim 27, wherein forming a first conductive layer includes depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer, the base conductive layer to provide at least one property, the property selected from an adhesion property and a barrier property.

29. (Withdrawn) The method of claim 28, wherein depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

30. (Withdrawn) The method of claim 27, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing material by ion implantation into the core conductive layer to form the capping ~~adhesion/barrier~~ layer.

31. (Withdrawn) The method of claim 27, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

32. (Withdrawn) The method of claim 27, wherein forming a first oxide layer above the device structures includes:

forming a field oxide layer and a Si_3N_4 layer above the one or more device structures;

forming contact holes through the field oxide layer and the Si_3N_4 layer;

depositing TiN in the contact holes;

forming tungsten on the TiN to form a contact plug; and

forming the first oxide layer on the Si_3N_4 layer and contact plug.

33. (Withdrawn) The method of claim 27, wherein forming a number of trenches in the first oxide layer includes:

forming a layer of Si_3N_4 on the first oxide layer;

applying a layer of resist;

forming a damascene image in the resist and Si_3N_4 layers; and

applying an oxide etch to define the number of trenches in the first oxide layer at locations of the damascene image.

34. (Withdrawn) The method of claim 33, wherein the method further includes after forming the first conductive layer removing the resist layer by a selective etch such that the first oxide layer is essentially unaltered by the selective etch.

35. (Withdrawn) The method of claim 27, wherein depositing a core conductive layer includes selectively depositing copper.

36. (Withdrawn) The method of claim 27, wherein depositing a core conductive layer includes selectively depositing the copper by plating in an ambient air environment.

37. (Withdrawn) The method of claim 27, wherein depositing ~~an adhesion/barrier~~ a capping layer on the core conductive layer includes implanting titanium ions into the core conductive layer.

38. (Withdrawn) The method of claim 37, wherein the method further includes exposing the titanium to nitrogen to form TiN.

39. (Withdrawn) The method of claim 27, wherein the method further includes removing at least a portion of the first oxide layer, after depositing the capping ~~adhesion/barrier~~ layer on the core conductive layer, to form an air bridge structure.

40. (Withdrawn) A method of forming a memory device comprising:

forming an array of memory cells in a substrate; and

forming a wiring structure in the substrate coupling to the array of memory cells, at least a portion of the wiring structure formed by a method including:

forming a first conductive layer in an opening in a multilayer dielectric structure supported by a substrate;

forming a core conductive layer on the first conductive layer, the core conductive layer having a top surface;

subjecting the core conductive layer to a H_2 plasma treatment; ~~and~~

depositing a capping ~~adhesion/barrier~~ layer on the core conductive layer after the H_2 plasma treatment, the capping layer to provide at least one property, the property selected from an adhesion property and a barrier property, the capping layer being conductive; and

processing the capping layer such that the capping layer completely covers the top surface of the core conductive layer substantially without being on areas surrounding the core conductive layer.

41. (Withdrawn) The method of claim 40, wherein forming a first conductive layer includes depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer, the base conductive layer to provide at least one property, the property selected from an adhesion property and a barrier property.

42. (Withdrawn) The method of claim 41, wherein depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

43. (Withdrawn) The method of claim 40, wherein forming a core conductive layer includes forming the core conductive layer at a temperature ranging from room temperature to about 250°C.

44. (Withdrawn) The method of claim 40, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

45. (Withdrawn) The method of claim 40, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing the capping ~~adhesion/barrier~~ layer having a thickness ranging from about 5 Å to about 40 Å.

46. (Withdrawn) The method of claim 40, wherein forming a core conductive layer and depositing a capping ~~adhesion/barrier~~ layer includes forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer in the opening in a multilayer dielectric structure such that the core conductive layer and the capping ~~adhesion/barrier~~ layer are within one dielectric layer in the multilayer dielectric structure with a top surface of the capping ~~adhesion/barrier~~ layer substantially level with a top surface of the one dielectric layer.

47. (Withdrawn) The method of claim 46, wherein forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer within one dielectric layer includes forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer within a polymer layer, a foamed polymer layer, a fluorinated polymer layer, an oxide layer, a silicon oxide layer, a fluorinated oxide layer, or an aerogel layer.

48. (Withdrawn) A method of forming an electronic system comprising:

providing a controller;

coupling the controller to one or more integrated circuits, at least the controller or one integrated circuit having a wiring structure on a substrate, at least a portion of the wiring structure formed by a method including:

forming a first conductive layer in an opening in a multilayer dielectric structure supported by a substrate;

forming a core conductive layer on the first conductive layer, the core conductive layer having a top surface;

subjecting the core conductive layer to a H_2 plasma treatment; ~~and~~

depositing a capping ~~adhesion/barrier~~ layer on the core conductive layer after the H_2 plasma treatment, the capping layer to provide at least one property, the property selected from an adhesion property and a barrier property, the capping layer being conductive; and

processing the capping layer such that the capping layer completely covers the top surface of the core conductive layer substantially without being on areas surrounding the core conductive layer.

49. (Withdrawn) The method of claim 48, wherein forming a first conductive layer includes depositing a seed layer on a ~~first adhesion/barrier~~ base conductive layer, the base conductive layer to provide at least one property, the property selected from an adhesion property and a barrier property.

50. (Withdrawn) The method of claim 49, wherein depositing a seed layer on a first ~~adhesion/barrier~~ base conductive layer includes depositing the seed layer on a layer of a refractory metal, a compound of nitrogen and a tantalum alloy, or a compound of nitrogen and a tungsten alloy.

51. (Withdrawn) The method of claim 48, wherein forming a core conductive layer includes forming the core conductive layer at a temperature ranging from room temperature to about 250°C.

52. (Withdrawn) The method of claim 48, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing one or more materials selected from titanium, zirconium, hafnium, and nitrides of these elements.

53. (Withdrawn) The method of claim 48, wherein depositing a capping ~~adhesion/barrier~~ layer includes depositing the capping ~~adhesion/barrier~~ layer having a thickness ranging from about 5 Å to about 40 Å.

54. (Withdrawn) The method of claim 48, wherein forming a core conductive layer and depositing a capping ~~adhesion/barrier~~ layer includes forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer in the opening in a multilayer dielectric structure such that the core conductive layer and the capping ~~adhesion/barrier~~ layer are within one dielectric layer in the multilayer dielectric structure with a top surface of the capping ~~adhesion/barrier~~ layer substantially level with a top surface of the one dielectric layer.

55. (Withdrawn) The method of claim 54, wherein forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer within one dielectric layer includes forming the core conductive layer and depositing the capping ~~adhesion/barrier~~ layer within a polymer layer, a foamed polymer layer, a fluorinated polymer layer, an oxide layer, a silicon oxide layer, a fluorinated oxide layer, or an aerogel layer.

56. (Withdrawn) The method of claim 48, wherein providing a controller includes providing a processor.

57. (Withdrawn) The method of claim 48, wherein forming the electronic system includes providing a computer.

58. – 103. (Cancelled)

104. (Previously Presented) The method of claim 1, wherein the method includes forming the electronic device configured as an integrated circuit.

105. (Previously Presented) The method of claim 1, wherein the method includes forming the electronic device configured as a memory device.

106. (Previously Presented) The method of claim 1, wherein the method includes forming the electronic device configured as part of an electronic system.